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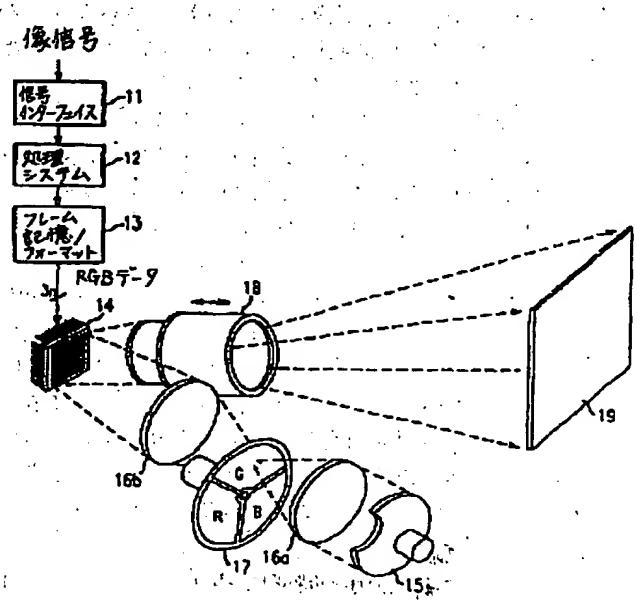
(54)【発明の名称】　イメージディスプレイシステムにおけるアーチファクト低減方法

(57)【要約】

【課題】　ＳＬＭベースディスプレイシステム内のアーチファクト低減方法を得る。

【解決手段】　ＳＬＭベースディスプレイシステム１０，２０の像はパルス幅変調された強度レベルに対してビットウェイトによりディスプレイされるデータに基づいている。この方法はさまざまなカラーの像を同時にディスプレイするマルチＳＬＭシステム２０や各フレーム期間中にさまざまなカラーの像を逐次発生するシングルＳＬＭシステム１０に使用することができる。マルチＳＬＭシステム２０に対しては、本方法はメモリ多重化された、さまざまな時間にロードされディスプレイされる“リセットグループ”を有するＳＬＭ１４に使用される。ＳＬＭの対応するローはさまざまなリセットグループと連関される。



1

【特許請求の範囲】

【請求項１】　多数のメモリ多重化空間光変調器（ＳＬＭ）を有し、各ＳＬＭが異なるカラーを表すピクセルデータに基づいた像をディスプレイし、像は像平面において結合されるイメージディスプレイシステムにおけるアーチファクト低減方法であって、該方法は、前記ＳＬＭ内に対応するロー位置を有する前記ＳＬＭのローを識別して対応するＳＬＭローを識別するステップと、各リセットグループが前記各ＳＬＭのいくつかのローからなりしかも対応するＳＬＭローが同じリセットグループ内には無いようにリセットグループ内の前記各ＳＬＭのローを接続するステップと、前記ピクセルデータのあるビットウェイトを有するデータを第１のリセットグループへロードするステップと、前記リセットグループへロードされた前記データをディスプレイするステップと、前記リセットグループ間で交互に各リセットグループおよび前記ピクセルデータの各ビットウェイトについて前記ローディングステップおよび前記ディスプレイステップを繰り返すステップとからなるアーチファクト低減方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はイメージディスプレイシステムに関し、特に１個以上の空間光変調器を使用してカラーディスプレイを発生するディスプレイシステムにおけるアーチファクト低減方法に関する。

【０００２】

【従来の技術】空間光変調器（ＳＬＭ：spatial light modolator）に基づいたイメージディスプレイシステムが陰極線管に基づいたイメージディスプレイシステムに代わるものとして次第に使用されつつある。イメージディスプレイ応用に使用されるＳＬＭは像平面へ光を放出もしくは反射するピクセル発生素子アレイである。画素と識別して、ピクセル発生素子自体を“ピクセル”と呼ぶことが多い。１つの画素を発生するのにＳＬＭアレイの２つ以上のピクセルを使用できることが判れば、この用語は前後関係から自明である。

【０００３】デジタルマイクロミラーデバイス（ＤＭＤ：digital micro-mirror device）はＳＬＭの１種である。ＤＭＤは数百乃至数千個の小さな傾斜ミラーのアレイを有している。傾斜できるようにするために、各ミラーは支柱に載置された１個以上のヒンジに取り付けられ、下層の制御回路から空隙により間隔がとられている。制御回路は静電力を与え、それにより各ミラーは選択的に傾斜する。各ミラー素子により１画素の強度が与えられる。

【０００４】所与の時間にどのピクセルをオンオフするかによって像が画定されるように、ＤＭＤのミラー素子を個別にアドレスすることができる。ＤＭＤのミラー素子をアドレスするために、各ミラー素子はアドレス信号のオンオフ状態を決定する少しのデータを記憶するメモリセルと連絡されている。ミラー素子が像平面へ光を反射するか否かを示すハイもしくはロー信号により各ミラー素子がアドレスされる点でアドレッシングはバイナリである。ミラー素子のＤＭＤアレイ周辺のデータローディング回路を介してメモリセル内に入力データを記憶することによりＤＭＤは“ロード”される。

2

【０００５】ピクセルデータは空間“ビットプレーン（bit-plane）”フォーマットでＤＭＤのメモリセルへ送られる。このフォーマットでは各フレームに対してデータはピクセル毎ではなく全ピクセルのビットウェイト（bit-weight）により配置される。このフォーマットでは１フレーム期間中に、各々がそのミラー素子のｎビットピクセル値の異なるビットウェイトを表す、連続アドレス信号により各ミラー素子をアドレスすることによりグレイスケール像を発生することができる。アドレッシングに使用されるビットのビットウェイトが上位であるほど、ミラー素子がオンのままとされる時間が長くなる。最も明るい強度に対しては、ミラー素子はアドレスされる度にオンとされる。これは本質的にパルス幅変調であり、多くのバリエーションが可能である。連続するフレームに対するデータによりＤＭＤを再アドレスすることにより移動像を発生することができる。

【０００６】カラーイメージに対する１つの方法は、各原色（Ｒ，Ｇ，Ｂ）について１個ずつの、３個のＤＭＤを使用することである。各ＤＭＤの対応するピクセルからの光は観察者が所望のカラーを知覚するように収束される。もう１つの方法は１個のＤＭＤと原色区画を有するカラーホイール（color wheel）を使用することである。さまざまなカラーに対するデータがカラーホイールへシーケンスされ同期化されて目の中でシーケンシャルな像が連続するカラー像へ統合されるようにされる。第３の方法では２個のＤＭＤが使用され、一方は２色間の切り替えに使用され、他方は第３色を表示するのに使用される。

【０００７】

【発明が解決しようとする課題】どんなディスプレイシステムでもそうであるが、ＤＭＤベースディスプレイシステムからの像の品質はアーチファクトを解消することにより改善される。潜在的なアーチファクトには観察者がまばたきしたり、目を動かしたり、目の前で手を振ったりした時にフラッシュや筋として現れる一時的な輪郭線が含まれる。もう１つのアーチファクトは動き輪郭線であり、それは移動物体を目で追っている時に疑似輪郭線として現れる。疑似輪郭線は急峻なエッジにおけるゴースト像もしくは緩やかに変化する領域におけるアーチファクト輪郭線である。メモリ多重化として知られるデータローディング法を使用するＤＭＤディスプレイシステムに特有な他種のアーチファクトもある。

【０００８】

【課題を解決するための手段】本発明の１つの特徴は多

数のメモリ多重化空間光変調器（ＳＬＭ）を有するイメージディスプレイシステム内のアーチファクト低減方法である。この種のシステムでは、各ＳＬＭは異なるカラーを表すデータに基づいた像を同時にディスプレイし、像は像平面において結合される。ＳＬＭは“対応する”ＳＬＭロー（raw ）を有し、それは対応するロー位置を有するローである。メモリ多重化のために、ＳＬＭのローはリセットグループ内で接続されている。各リセットグループは各ＳＬＭのいくつかのローからなり、対応するＳＬＭローは同じリセットグループ内には無い。ＳＬＭへデータをローディングする間に、第１のリセットグループにはピクセルデータの、あるビットウェイトを有するデータがロードされる。このデータは、次のリセットグループにピクセルデータの、あるビットウェイトを有するデータがロードされる間に、ディスプレイされる。これらのローディングおよびディスプレイステップは各リセットグループおよびピクセルデータの各ビットウェイトに対して繰り返される。

【０００９】本発明の利点はリセットグループが対応するＳＬＭローを含んでいないため、スプリットリセット構成の周期性によるアーチファクトが低減されることである。例えば、スプリットリセット構成が水平であれば、水平線構造を知覚する傾向が少なくなる。

【００１０】本発明は１個のＳＬＭを使用してカラーホイールを介したさまざまなカラーの像を逐次表示するシングルＳＬＭシステムにも有用である。この場合、１組のＳＬＭローしかない。１つのカラーに対するリセットグループは別のカラーに対するリセットグループとは異なるローを有している。

【００１１】

【発明の実施の形態】図１および図２は、それぞれ、ＳＬＭに基づくカラーディスプレイシステム１０および２０のブロック図である。システム１０はカラーホイールを介したさまざまなカラーの像を逐次ディスプレイする１個のＳＬＭを使用している。システム２０は３個のＳＬＭを使用し、その各々が像の異なるカラーに対するデータを同時にディスプレイする。後記するように、カラーディスプレイがシステム１０のように逐次与えられるかシステム２０のように同時に与えられるかに拘わらず、各システムは多数のデータチャネルを有し、各チャネルが異なるカラー用とされている。一般的に、本発明はさまざまなチャネルのデータのタイミングを変えてディスプレイされる像内のアーチファクトを低減するものである。

【００１２】例えば、システム１０のＳＬＭ１４およびシステム２０のＳＬＭ１４はＤＭＤ型ＳＬＭである。後記するように、本発明ではメモリ多重化ＳＬＭが使用される。ＳＬＭがＤＭＤである場合には、リセットされるまでオンもしくはオフ位置に設定されたままとされる傾斜ミラーのラッチング特性によりこのメモリ多重化が可

能とされる。この特性により、１組のミラー素子が既に設定されている時にもう１組のミラー素子を関連するメモリセルへロードすることができる。これによりミラー素子はメモリセルを共有することができる。

【００１３】システム１０やシステム２０が受信するイメージ信号はデジタル信号もしくは後にデジタル形式に変換されるアナログ信号とすることができる。例えば、入信号は放送されたテレビジョン信号のようなアナログ信号と考えることができる。

【００１４】図１および図２には、主画面処理にとって重要な構成要素しか示されていない。同期化およびオーディオ信号の処理やクローズドキャプショニング（closed captioning ）等の機能に使用される他の構成要素は示されていない。

【００１５】システム１０およびシステム２０は“フロントエンド”構成要素と同じような構成を有し、ＤＭＤ１４へデジタル像データを与えるための、信号インターフェイス１１、処理システム１２、およびフレームメモリ１３、を含む。これらの構成要素についてはシステム１０およびシステム２０に対して共通に検討し、ＤＭＤ１４および２つのシステムの関連する光学系については別々に検討する。システム１０およびシステム２０を共通に検討する場合には、ＤＭＤはシステム１０の１個のＤＭＤもしくはシステム２０の多数のＤＭＤ１４を表す。

【００１６】信号インターフェイス１１はアナログ入力信号を受信し、ビデオ信号、同期信号、およびオーディオ信号に分離する。信号インターフェイス１１は、それぞれ、信号をピクセルデータへ変換しクロミナンスデータから輝度データを分離する、Ａ／Ｄコンバータおよびカラーセパレータを含んでいる。別の実施例では、カラー分離はＡ／Ｄ変換を行う前にアナログフィルタを使用して行われる。

【００１７】プロセッサシステム１２はさまざまなピクセル処理タスクを実施することによりディスプレイするピクセルデータを準備する。プロセッサシステム１２は処理中にピクセルデータを格納する、フィールドおよびラインバッファ等の、さまざまなメモリデバイスを含んでいる。

【００１８】プロセッサシステム１２により代表的に実施される１つのタスクはインターレースされたデータの前進走査変換であり、インターレースされたデータの各フィールドが完全なフレームへ変換される。他の処理タスクはスケーリング、色空間変換、もしくはガンマ補正である。色空間変換中に、輝度およびクロミナンスデータはＲＧＢデータへ変換される。ＤＭＤ１４の線形特性によりガンマ補償は不要となるためガンマ補正によりガンマ補償されたデータは逆補償される。

【００１９】実施例では、プロセッサシステム１２は前進走査変換およびスケーリング等の計算処理タスクを実

施する“走査線ビデオプロセッサ”を含んでいる。このデバイスはテキサスインスツルメンツ社から市販されており、ピクセルデータのラインバイライン処理を行うことができる。

【００２０】フレームメモリ１３はプロセッサシステム１２から処理されたピクセルデータを受信する。フレームメモリ１３は、入力もしくは出力において、データを“ビットプレーン”フォーマットへ変換し、ビットプレーンデータをDMDへ送る。従来の技術で検討したように、ビットプレーンフォーマットはピクセルデータがビットウェートにより再構成されるフォーマットである。これによりDMD１４の各ピクセルはある時間の１ビットデータの値に応答してオンオフすることができる。

【００２１】代表的なディスプレイシステム１０では、フレームメモリ１３は“ダブルバッファ”メモリであり、少なくとも２つのディスプレイフレームに対する容量を有することを意味する。一方のディスプレイフレームに対するバッファへ書き込んでいる間に他方のディスプレイフレームに対するバッファをDMD１４へ読み出すことができる。２個のバッファは“ピンポン”式に制御してDMD１４は連続的にデータを得ることができる。

【００２２】従来の技術で前記したように、DMD１４は各ミラー素子のオンオフ状態を有する２進デバイスである。データの各ビットに対するビットプレーンはパルス幅変調シーケンスによりロードされディスプレイされる。ｎビットピクセルデータに対しては、フレーム期間当たりｎビットプレーンがある。フレーム期間中に、観察者は２進データを統合してそのフレームの像のさまざまな強度を知覚する。

【００２３】次に図１およびシステム１０を参照して、DMD１４へのＲＧＢデータの各フレームへ一時に１つのカラーが与えられ、データの各フレームがレッド、ブルー、およびグリーンのデータセグメントへ分割されるようにされる。各セグメントのディスプレイ時間はフレーム毎に１回転するカラーフォイール１７に同期化され、DMD１４が適切な時間にカラーフォイール１７を介した１つのカラーに対するデータを表示するようにされる。したがって、各カラー（Ｒ，ＧおよびＢ）に対するデータチャネルは各フレームがさまざまなカラーに対するシーケンシャルデータを有するように時間多重化される。

【００２４】シーケンシャルカラーシステム１０に対して、光源１５から集光レンズ１６ａを介して白色光が送られ、それは回転するカラーフォイール１７上の一点へ収束される。第２のレンズ１６ｂによりカラー光線はDMDのミラーアレイのサイズへ適合される。DMDからの反射光により画面１９上に像が投影される。投影レンズ１８はさまざまな画面サイズに調整される。

【００２５】図２およびシステム２０を参照して、Ｒ，

ＧおよびＢデータについて１つづつの３つの異なるデータパスに沿って３個のDMD１４へデータが与えられる。光源１６から集光レンズ２６ａを介して白色光が送られ、それはカラーフィルタ２７を介して収束される。各カラーフィルタ２６は異なるカラーの光（Ｒ，ＧおよびＢ）をDMD１４へ与え、そのカラーに対するデータがディスプレイされる。フィルタ２６ｂによりDMD１４からの像が再結合されて投影レンズ１８上へ収束され、画面１９へ像が収束される。システム２０の１つのバリエーションでは１個の大型DMDが各カラーに対する領域を有している。

【００２６】システム１０およびシステム２０のようなシーケンシャルカラーおよびマルチDMDシステムの両方に対する包括的な説明がテキサスインスツルメンツ社が譲り受けたいくつかの特許および特許出願に記載されている。それには米国特許第５，０７９，５４４号“標準独立デジタル化ビデオシステム”、米国特許第５，２３３，３８５号“白色光強化カラーフィールドシーケンシャル投影”、米国特許出願第０７／６７８，７６１号“パルス幅変調ディスプレイシステムに使用するDMDアーキテクチュアおよびタイミング”、米国特許出願第０８／１４７，２４９号“デジタルテレビジョンシステム”、および米国特許出願第０８／１４６，３８５号“DMDディスプレイシステム”が含まれる。これらの各特許および特許出願がここに組み入れられている。

【００２７】本発明の特徴はビットプレーンディスプレイにより遷移エネルギ変化が生じることを認識することである。ビットプレーンディスプレイでは、特別なデータシーケンスによりピクセルの各ビットウェートについてディスプレイ時間の順序、すなわちディスプレイ時間のセグメント、が指定される。単純な例として、８ビットピクセルデータに対するシーケンスは７，６，５，４，３，２，１，０とすることができ、各ビットウェートに対するディスプレイ時間はフレーム中に順次短かくなる。１つのビットレベルからもう１つのビットレベルへの遷移毎に遷移エネルギが関連している。高い遷移エネルギはアーチファクトとして知覚することができる。

【００２８】ピークエネルギレベルを低減する１つの方法はビットウェートを“分割”して各高いビットウェートに対するディスプレイ時間が連続的ではなくフレーム期間中にセグメント化されるようにすることである。例えば、最上位ビットに対するディスプレイ時間は２つの部分へ分割することができる。次に、最上位ビット（ＭＳＢ）に対するデータがフレーム期間中に２度ディスプレイされ、その各オン時間は総ＭＳＢ時間の半分である。

【００２９】図３に前記したビット分割方法の替わりとしてもしくはそれを補足するために使用することができるディスプレイシーケンス方法を示す。この方法ではアーチファクトを低減するように遷移エネルギが分散され

る。

【００３０】図３の例では、この方法はシステム２０等のマルチＳＬＭシステムに実施される。各ＤＭＤ１４はレッド、グリーン、もしくはブルーデータを受信し、したがって各々がＤＭＤ１４－Ｒ、１４－Ｇ、もしくは１４－Ｂとして示されている。

【００３１】図３のＤＭＤ１４は各々がメモリ多重化されている。前記したように、これは多数のミラー素子に同じメモリセルからデータがロードされることを意味する。メモリセルを共有する各ミラー素子が異なるリセット線に接続されている。全体ＤＭＤに対して、メモリセル当たりミラー素子と同数のリセット線がある。特定のリセット線に接続されたミラー素子は“リセットグループ”である。動作について、ミラー素子のリセットグループに対する全メモリセルにデータがロードされた後で、これらのミラー素子の状態はそのリセット線上のリセット信号に応答して変化する。メモリの多重化とそれに伴う“スプリットーリセット”データローディング方式についてはテキサスインスツルメンツ社が譲り受け参照としてここに組み入れられている米国特許出願第０８／３００／３５６号“空間光変調器用ピクセル制御回路”に記載されている。

【００３２】ここに記載する例では、メモリ多重化はロー（raw）（水平の）によるものであり１つのメモリセルからのミラー素子のファンアウトは４である。したがって、ミラー素子の連続する４ロー毎に１ローのメモリセルが共有される。メモリセルを共有する４ローのミラー素子は１“ブロック”のミラー素子である。４８０ローのミラー素子を有するＤＭＤ１４は１２０のブロック４１を有する。各ブロック４１は４ローを有し、それらはメモリセルの同じローからデータを受信する。

【００３３】代表的なメモリ多重化構成と同様に、各ローは４本のリセット線の１本に接続されている。図４には、１本のリセット線４２しか示されていないが４本のリセット線がある。リセット線４２は３個のＤＭＤ１４の全ブロックの第１ローを含むリセットグループに接続される。したがって、リセットグループは全ＤＭＤ１４のロー数の１／４を含んでいる。

【００３４】リセットグループへのデータは１タイムスライス中にロードされる。次のリセットグループへのデータがロードされている間に、第１のリセットグループのミラー素子はリセット信号に応答してオンオフされる。

【００３５】より詳細には、フレームのデータローディング中に、同じブロックロー番号を有するローからなるリセットグループがフレーム期間のタイムスライス中にビットウェートによりロードされる。“タイムスライス”はフレーム期間の一部であり、最下位ビットに対するディスプレイ期間である場合が多い。タイムスライスは短すぎて余分なタイムスライスが許されない場合もあるが、一般的には、最下位ビットの持続時間により決定される。

【００３６】１フレームのデータをローディングしてメモリ多重化システム２０上へディスプレイする１例として、第１のリセットグループのビットｎがロードされ、次に第２のリセットグループのビットｎがロードされ、次に第３のリセットグループのビットｎがロードされ、次に第４のリセットグループのビットｎがロードされる。次に、第１のリセットグループのビットｎ－１がロードされ、次に第２のリセットグループのビットｎ－１がロードされ、以下全リセットグループの全ビットウェートがロードされるまで続けられる。各リセットグループ／ビットウェイトに対するデータがロードされると、前のリセットグループ／ビットウェイトデータがディスプレイされる。この例では、ビットウェートは各リセットグループに対して同じ順序に従うが、これは要求されているわけではない。事実、リセットグループの中では、さまざまなビットウェートシーケンスが有利である。このようにして、各フレーム期間中に、全ＤＭＤローがそれらのリセットグループを介して、またそのフレームに対するデータの全ビットウェートがロードされてディスプレイされる。

【００３７】システム２０等のメモリ多重化ディスプレイシステムに対しては、画像品質を最適化する特殊なローディングおよびディスプレイパターンが開発されている。図３の例では、次のようなパターンとすることができる。

リセットグループ１、ビットウェートシーケンスａ
リセットグループ２、ビットウェートシーケンスｂ
リセットグループ３、ビットウェートシーケンスｃ
リセットグループ４、ビットウェートシーケンスｄ

前記したように、ローディングおよびディスプレーイング中に、各シーケンスのビットウェートはリセットグループ間で変更される。

【００３８】図３のＤＭＤ１４が“対応する”ローを有しており、各ＤＭＤ１４の第ｎローが各ＤＭＤ１４についてその同じ位置にある。したがって、“１”とマークされた各ＤＭＤ１４の第１のＤＭＤローがディスプレイされるデータの第１ローを受信する。これら３つのローは対応するローである。同様に、４８０ロー像に対する、各ＤＭＤ１４の第４８０番ローはディスプレイされるデータの最終ローを受信する。これらの３つの第４８０番ローは対応するローである。

【００３９】図からお判りのように、ＤＭＤ１４のＤＭＤローとそのブロックロー間の連関はＤＭＤ１４間で垂直にオフセットされている。すなわち、ＤＭＤ１４の所与の１組の対応するローに対して、各ＤＭＤローは異なるブロックローと連関されている。例えば、ＤＭＤ１４－Ｒの第１のローはブロック４１－Ｒ（１）の第１のローと連関されている。しかしながら、ＤＭＤ１４－Ｇの

第１のローはブロック４１－Ｇ（１）の第４ローに対応している。ＤＭＤ１４－Ｂの第１のローはブロック４１－Ｂ（１）の第３ローに対応している。

【００４０】前記したことと一貫して、第１のリセットグループに対しては、連関するＤＭＤローはＤＭＤ１４－Ｒの１，５，９．．．４７７ロー、ＤＭＤ１４－Ｇの２，６，１０，．．．４７８ロー、およびＤＭＤ１４－Ｂの３，７，１１，．．．４７９ローである。各リセットパターンは同様なパターンで接続されており、ＤＭＤローは対応するＤＭＤローが同じリセットグループ内には無いように接続されている。

【００４１】前記したように、ディスプレイはミラー素子のリセットグループをローディングしかつリセットすることにより発生される。特定のリセットグループがディスプレイされると、連関するＤＭＤローは対応しない。例えば、リセット線４２に接続されたリセットグループがディスプレイされる場合、ディスプレイされるＤＭＤローはＤＭＤ１４－Ｒの１，５，９，．．．４７７ロー、ＤＭＤ１４－Ｇの２，６，１０，．．．４７８ロー、およびＤＭＤ１４－Ｂの３，７，１１，．．．４７９ローである。

【００４２】対応するＤＭＤローとリセットグループ間の連関が非均一であるため、各カラーに対するデータは同じパターンに従うことができる。しかしながら、各カラーに対する遷移時間が異なるため遷移ピークが低減される。

【００４３】対応するＤＭＤローを異なるリセットグループと連関させる前記方法は水平メモリ多重化ＤＭＤ１４に向けられたものであるが、同じ概念を他のメモリ多重化構成に応用することができる。例えば、メモリ多重化は対角とすることができる。水平メモリ多重化の場合のように、各メモリセルのファンアウトは１組の垂直に連続するミラー素子である。しかしながら、ブロックローは対角線に沿っており、ブロックローｎに対するデータはＤＭＤロー１のピクセル１、ＤＭＤロー２のピクセル４、ＤＭＤロー３のピクセル３、およびＤＭＤロー４のピクセル２等に対するデータを含むことがある。ｎローを有するＤＭＤに対しては、２ｎ－１のブロックローがある。対角メモリ多重化についてはここに組み入れられている米国特許出願第０８／３００，３５６号に詳細に記載されている。

【００４４】図４は本発明に従って対角分割リセットを行うように構成された３個のＳＬＭの８ｘ８ピクセル部を示す。異なるリセットグループに対して１本づつの４本のリセット線４２がある。ＳＬＭ１４の対応する４組の対角ローが示されている。各ＤＭＤ１４の対応する対角ローはさまざまなリセットグループと連関されている。

【００４５】同じ概念が２個のＤＭＤしかないシステムに応用される。さらに、システム１０等のシングルＤＭＤシステムに対しては、ＤＭＤローとリセットグループ間の対応はカラー毎にシフトさせて図３の方法のシーケンシャルバージョンを実現することができる。各カラーに対して、リセットグループを再構成してさまざまなＳＬＭローを含む用にすることができる。目の積分（eye's integration）はフレーム期間内のエネルギの積分に基づいているため、フレーム期間内でエネルギレベルを適切に分散させることによりアーチファクトを低減することができる。

【００４６】特定の実施例について本発明を説明してきたが、本明細書は制約的意味合いを有するものではない。当業者であれば他の実施例だけでなく開示された実施例のさまざまな改良が容易にお判りと思われる。したがって、発明の真の範囲内に入る改良は全て特許請求の範囲に入るものとする。

【００４７】以上の説明に関して更に以下の項を開示する。

（１）．多数のメモリ多重化空間光変調器（ＳＬＭ）を有し、各ＳＬＭが異なるカラーを表すピクセルデータに基づいた像をディスプレイし、像は像平面において結合されるイメージディスプレイシステムにおけるアーチファクト低減方法であって、該方法は、前記ＳＬＭ内に対応するロー位置を有する前記ＳＬＭのローを識別して対応するＳＬＭローを識別するステップと、各リセットグループが前記各ＳＬＭのいくつかのローからなりしかも対応するＳＬＭローが同じリセットグループ内には無いようにリセットグループ内で前記各ＳＬＭのローを接続するステップと、前記ピクセルデータの、あるビットウェイトを有するデータを第１のリセットグループへロードするステップと、前記第１のリセットグループへロードされた前記データをディスプレイするステップと、前記リセットグループ間で交互に各リセットグループおよび前記ピクセルデータの各ビットウェイトについて前記ローディングステップおよび前記ディスプレイステップを繰り返すステップとからなるアーチファクト低減方法。

【００４８】（２）．第１項記載の方法であって、前記対応するローの各ローが異なるリセットグループ内にあるアーチファクト低減方法。

【００４９】（３）．第１項記載の方法であって、前記繰り返しステップは前記ビットウェイトがさまざまなリセットグループに対してさまざまな順序でロードされるように実施されるアーチファクト低減方法。

【００５０】（４）．第１項記載の方法であって、前記ローディングステップおよび前記ディスプレイステップはフレーム期間の２つの連続するタイムスライス内で実施され、前記タイムスライスは実質的に最下位ビットウェイトを有するデータに対するディスプレイ時間により決定されるアーチファクト低減方法。

【００５１】（５）．第１項記載の方法であって、前記

ＳＬＭディスプレイデータの１つは２つのカラーに対するものであり前記ＳＬＭデータの１つは第３のカラーに対するものであるアーチファクト低減方法。

【００５２】（６）．第１項記載の方法であって、前記各ＳＬＭディスプレイデータが異なるカラーに対するものであるアーチファクト低減方法。

【００５３】（７）．第１項記載の方法であって、前記ＳＬＭはデジタルマイクロミラーデバイスであるアーチファクト低減方法。

【００５４】（８）．第１項記載の方法であって、前記対応するローは前記ＳＬＭの水平ローに沿っておりリセットグループは前記水平ローを含むアーチファクト低減方法。

【００５５】（９）．第１項記載の方法であって、前記対応するローは前記ＳＬＭの対角ローに沿っており前記リセットグループは前記対角ローを含むアーチファクト低減方法。

【００５６】（１０）．メモリ多重化空間光変調器（ＳＬＭ）を有し、カラーフォイールを介し、異なるカラーを表すピクセルデータに基づいた像を逐次ディスプレイする、イメージディスプレイシステムにおけるアーチファクト低減方法であって、該方法は、各リセットグループが前記ＳＬＭのいくつかのローからなるようにリセットグループへ前記ＳＬＭのローを割り当てるステップと、前記ピクセルデータの、あるビットウェイトを有するデータを第１のリセットグループへロードするステップと、前記第１のリセットグループへロードされた前記データをディスプレイするステップと、前記リセットグループ間で交互に各リセットグループおよび第１のカラーの前記ピクセルデータの各ビットウェイトについて前記ローディングステップおよび前記ディスプレイステップを繰り返すステップと、前記リセットグループが前記ＳＬＭのさまざまなローを含むように第２のカラーの前記ピクセルデータについて前記割り当て、ローディング、およびディスプレイステップを繰り返すステップとからなるアーチファクト低減方法。

【００５７】（１１）．第１０項記載の方法であって、前記繰り返しステップは前記ビットウェイトがさまざまなリセットグループに対してさまざまな順序でロードされるように実施されるアーチファクト低減方法。

【００５８】（１２）．第１０項記載の方法であって、前記ローディングステップおよび前記ディスプレイステップはフレーム期間の２つの連続するタイムスライス内で実施され、前記タイムスライスは実質的に最下位ビットウェイトを有するデータに対するディスプレイ時間により決定されるアーチファクト低減方法。

【００５９】（１３）．第１０項記載の方法であって、

前記リセットグループは前記ＳＬＭの対角ローを含むアーチファクト低減方法。

【００６０】（１４）．第１０項記載の方法であって、前記リセットグループは前記ＳＬＭの水平ローを含むアーチファクト低減方法。

【００６１】（１５）．第１０項記載の方法であって、前記ＳＬＭはデジタルマイクロミラーデバイスであるアーチファクト低減方法。

【００６２】（１６）．ＳＬＭに基づいたディスプレイシステム１０，２０内のアーチファクト低減方法であって、その像はパルス幅変調された強度レベルに対してビットウェイトによりディスプレイされるデータに基づいている。この方法はさまざまなカラーの像を同時にディスプレイするマルチＳＬＭシステム２０や各フレーム期間中にさまざまなカラーの像を逐次発生するシングルＳＬＭシステム１０に使用することができる。マルチＳＬＭシステム２０に対しては、本方法はメモリ多重化された、さまざまな時間にロードされディスプレイされる“リセットグループ”を有するＳＬＭ１４に使用される。ＳＬＭの対応するローはさまざまなリセットグループと連関付けられている。

【図面の簡単な説明】

【図１】１個のＳＬＭおよびカラーフォイールを使用してカラー像を与えるＳＬＭベースディスプレイシステムのブロック図。

【図２】多数のＳＬＭを使用してカラー像を与えるＳＬＭに基づくディスプレイシステムのブロック図。

【図３】水平メモリ多重化ＳＬＭを有する、図２のシステム内のアーチファクトを低減する方法を示す図。

【図４】対角にメモリ多重化されるＳＬＭに対する方法を示す図。

【符号の説明】

１０，２０　ＳＬＭに基づくカラーディスプレイシステム

１１　信号インターフェイス

１２　処理システム

１３　フレームメモリ

１４，１４Ｒ，１４－Ｂ，１４－Ｇ　デジタルミラーデバイス

１５　光源

１６ａ，１６ｂ　レンズ

１７　カラーフォイール

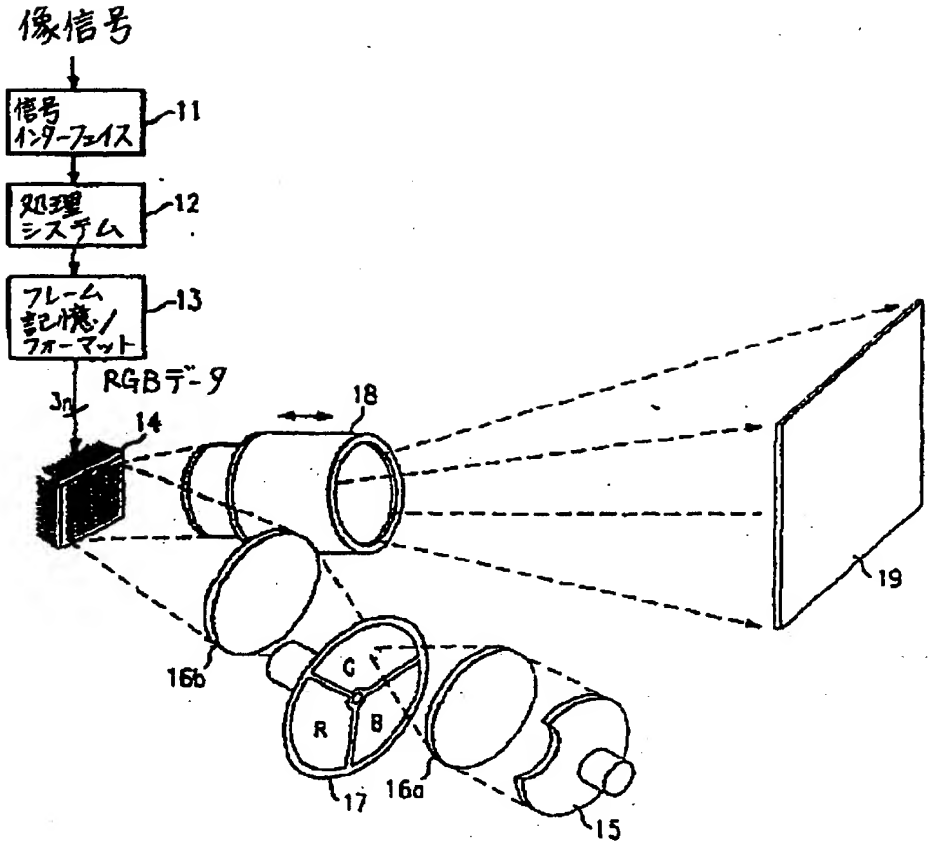
１８　投影レンズ

１９　画面

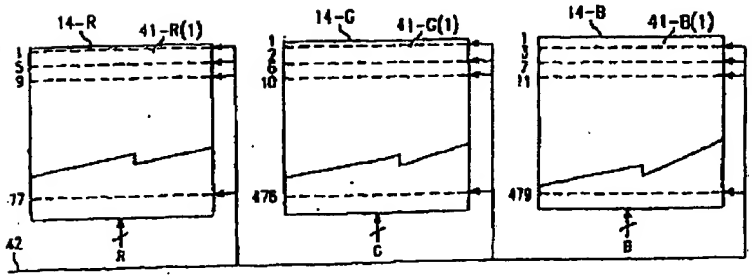
２６ａ，２６ｂ　集光レンズ

２７　カラーフィルタ

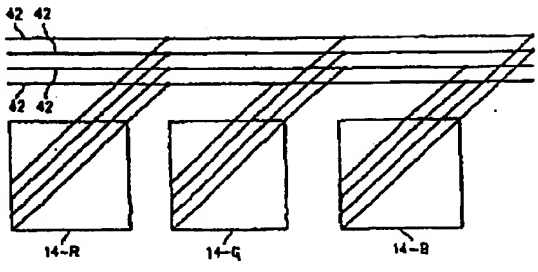
【図１】


像信号
信号インターフェイス
11
処理システム
12
フレーム記憶/フォーマット
13
RGBデータ
3n
14
18
19
16b
16a
15
17
R
G
B

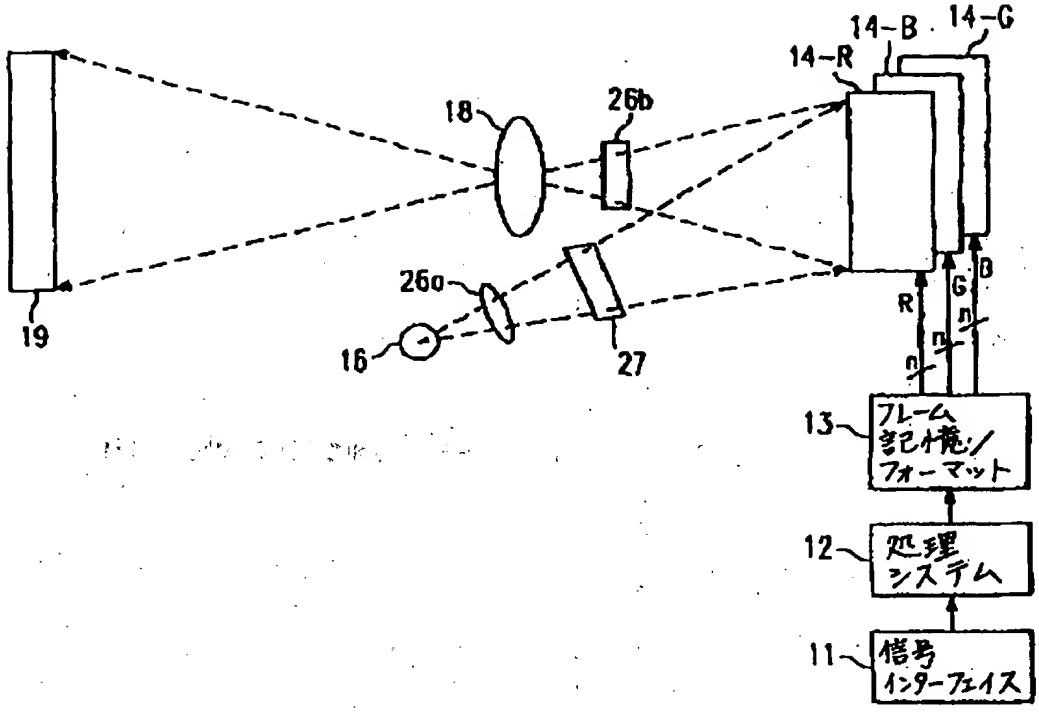
【図３】


14-R
41-R(1)
14-G
41-G(1)
14-B
41-B(1)
1
5
9
477
476
2
6
10
3
7
11
479
42
R
G
B

【図４】


42
RG1
RG2
RG3
RG4
14-R
14-G
14-B

【図２】


14-B
14-G
14-R
18
26b
26a
19
16
27
R
G
B
n
n
n
13
フレーム
記憶/
フォーマット
12
処理
システム
11
信号
インターフェイス

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] Have many memory multiplexing space optical modulators (SLM), and the image based on the pixel data showing each color from which SLM differs is displayed. An image is the artifact reduction approach in the image display system combined in an image plane. This approach The step which identifies the SLM low which identifies said low of SLM which has a low location [/ in said SLM], and corresponds, each reset group — said every — there is no SLM low which consists of some lows of SLM and moreover corresponds into the same reset group — as — said every in a reset group — with the step which connects the low of SLM The step which loads the data which have a bit wait with said pixel data to the 1st reset group, The step which displays said data loaded to said reset group, The artifact reduction approach which consists of a step which repeats said loading step and said display step by turns among said reset groups about each reset group and each bit wait of said pixel data.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the artifact reduction approach in the display system which generates a color display especially using one or more space optical modulators about an image display system.
[0002]
[Description of the Prior Art] It is gradually used as what the image display system based on a space optical modulator (SLM:spatial light modolator) replaces with the image display system based on a cathode-ray tube. SLM used for image display application is a pixel generating component array which emits or reflects light in an image plane. It discriminates from a pixel and the pixel generating component itself is called a "pixel" in many cases. If it turns out that two or more pixels of a SLM array can be used for generating one pixel, this vocabulary is obvious from a context.
[0003] A digital micro mirror device (DMD:digital micro-mirror device) is one sort of SLM. DMD has the array of hundreds thru/or thousands of small inclination mirrors. Since it enables it to incline, each mirror is attached in one or more hinges laid in the stanchion, and spacing is taken by the opening from the lower layer control circuit. A control circuit gives electrostatic force and, thereby, each mirror inclines alternatively. The reinforcement of 1 pixel is given by each mirror component.
[0004] The address of the mirror component of DMD can be carried out according to an individual so that an image may be demarcated by which pixel is turned on and off to given time amount. In order to carry out the address of the mirror component of DMD, each mirror component is connected with the memory cell which memorizes a little data which determine the on-off condition of an address signal. Addressing is binary at the point that the address of each mirror component is carried out by the yes or low signal which shows whether a mirror component reflects light in an image plane. DMD "is loaded" by memorizing input data in a memory cell through the data loading circuit of the DMD array circumference of a mirror component.
[0005] Pixel data are sent to the memory cell of DMD in a space "bit plane (bit-plane)" format. In this format, data are arranged by the bit wait (bit-weight) of every pixel and all pixels to each frame. In this format, a gray scale image can be generated by carrying out the address of each mirror component during an one-frame period with the consecutive-addresses signal with which each expresses the bit wait from which the n bit pixel value of that mirror component differs. The time amount it is supposed that a mirror component continues being ON becomes long, so that the bit wait of the bit used for addressing is a high order. To the brightest reinforcement, whenever the address of the mirror component is carried out, it is set to ON. This is essentially pulse width modulation and many variations are possible for it. A migration image can be generated by carrying out the re-address of the DMD with the data to a continuous frame.
[0006] One approach for a color image is using three DMD(s) per piece about each primary color (R, G, B). It converges the light from each pixel to which DMD corresponds so that an observer may perceive a desired color. Another approach is using the color wheel (color wheel) which has

one DMD and primary color partition. It is made to be unified to the color image with which the sequence of the data to various colors is carried out, they are synchronized to a color wheel, and a sequential image continues in an eye. By the 3rd approach, two DMD(s) are used, one side is used for the change between 2 colors, and it is used for another side displaying the 3rd color.
[0007]
[Problem(s) to be Solved by the Invention] With any display systems, although that is right, the quality of the image from a DMD base display system improves by canceling the artifact. When an observer winks to the potential artifact, an eye is moved or a hand is shaken in front of an eye, a temporary border line which appears as a flash plate or a muscle is contained. Another artifact is a motion border line, and it appears as a false border line, when having run after the migration body by the eye. A false border line is a ghost image in a steep edge, or an artifact border line in the field which changes gently. There is also artifact of other type peculiar to the DMD display system which uses the data loading method learned as memory multiplexing.
[0008]
[Means for Solving the Problem] One description of this invention is the artifact reduction approach in the image display system which has many memory multiplexing space optical modulators (SLM). In this kind of system, each SLM displays the image based on the data showing a different color in coincidence, and an image is combined in an image plane. SLM has a "corresponding" SLM low (raw) and it is a low which has a low corresponding location. For memory multiplexing, the low of SLM is connected within the reset group. Each reset group consists of some of each lows of SLM, and there is no corresponding SLM low into the same reset group. While carrying out loading of the data to SLM, the data which have a certain bit wait of pixel data are loaded to the 1st reset group. This data is displayed while the data which have a certain bit wait of pixel data are loaded to the next reset group. These loading and a display step are repeated to each reset group and each bit wait of pixel data.
[0009] Since the advantage of this invention does not contain the SLM low to which a reset group corresponds, it is that the artifact by the periodicity of a split reset configuration is reduced. For example, if the split reset configuration is level, the inclination to perceive horizontal line structure will decrease.
[0010] This invention is useful also to the single SLM system which displays serially the image of various colors which minded the color wheel using one SLM. In this case, there are only 1 set of SLM lows. The reset group to one color has a different low from the reset group to another color.
[0011]
[Embodiment of the Invention] Drawing 1 and drawing 2 are the block diagrams of the color display systems 10 and 20 based on SLM, respectively. The system 10 is using one SLM which displays the image of various colors through a color wheel serially. A system 20 uses three SLM (s) and the each displays in coincidence the data to the color from which an image differs. Irrespective of whether a color display is serially given like a system 10, or it is given to coincidence like a system 20, each system has many data channels and is made into the colors from which each channel differs so that a postscript may be carried out. Generally, this invention reduces the artifact in the image displayed by changing the timing of the data of various channels.
[0012] For example, SLM14 of a system 10 and SLM14 of a system 20 are the DMD molds SLM. In this invention, the memory multiplexing SLM is used so that a postscript may be carried out. When SLM is DMD, this memory multiplexing is enabled by the latching property of the inclination mirror it is supposed that is set as ON or an off position until it is reset. With this property, when 1 set of mirror components are already set up, 1 more set of mirror components can be loaded to a related memory cell. Thereby, a mirror component can share a memory cell.
[0013] The image signal which a system 10 and a system 20 receive can be made into the analog signal changed into a digital format in a digital signal or the back. For example, a conversion number can be considered to be an analog signal like the broadcast television signal.
[0014] Only the component important for the main screen processing is shown in drawing 1 and drawing 2 . Other components used for functions, such as synchronization and processing of an

audio signal, and closed KYAPUSHONINGU (closed captioning), are not shown.
[0015] A system 10 and a system 20 have the same configuration as a "front end" component, and contain the signal interface 11, the processing system 12, and frame memory 13 for giving digital image data to DMD14. These components are examined in common to a system 10 and a system 20, and the optical system to which DMD14 and two systems relate is examined separately. In examining a system 10 and a system 20 in common, DMD expresses much DMD14 of one DMD of a system 10, or a system 20.
[0016] The signal interface 11 receives an analog input signal, and divides it into a video signal, a synchronizing signal, and an audio signal. The signal interface 11 contains the A/D converter and color separator which change a signal into pixel data and separate brightness data from chrominance data, respectively. In the another example, before color separation performs A/D conversion, it is performed using an analog filter.
[0017] The processor system 12 prepares the pixel data displayed by carrying out various pixel processing tasks. The processor system 12 contains various memory devices, such as the field, a line buffer, etc. which store pixel data during processing.
[0018] One task typically carried out by the processor system 12 is advance scan conversion of the interlaced data, and each field of the interlaced data is changed into a perfect frame. Other processing tasks are a scaling, a color space conversion, or a gamma correction. Brightness and chrominance data are changed into RGB data into a color space conversion. Since gamma compensation becomes unnecessary with the linearity property of DMD14, the data in which gamma compensation was carried out by the gamma correction are reverse-compensated.
[0019] In the example, the processor system 12 contains the "scanning-line video processor" which carries out computation tasks, such as advance scan conversion and a scaling. This device is marketed from Texas Instruments, Inc., and can perform line BAIRAIN processing of pixel data.
[0020] A frame memory 13 receives the pixel data processed from the processor system 12. In an input or an output, a frame memory 13 changes data into a "bit plane" format, and sends bit plane data to DMD. As the Prior art examined, a bit plane format is a format pixel data are reconfigurated by whose bit wait. Thereby, each pixel of DMD14 can answer the value of 1 bit data of a certain time amount, and can be turned on and off.
[0021] With the typical display system 10, a frame memory 13 is "double buffer" memory, and it means having the capacity to at least two display frames. While writing in the buffer to one display frame, the buffer to the display frame of another side can be read to DMD14. Two buffers can be controlled at a "ping-pong" ceremony, and DMD14 can obtain data continuously.
[0022] As described above by the Prior art, DMD14 is a binary device which has the on-off condition of each mirror component. The bit plane to each bit of data is loaded by the pulse-width-modulation sequence, and is displayed. To n bit pixel data, there is an n bit plane per frame period. During a frame period, an observer unifies binary data and perceives various reinforcement of the image of the frame.
[0023] Next, one color is given at a stretch to each frame of the RGB data to DMD14, and it is made to be divided in each frame of data with reference to drawing 1 and a system 10 to red, blue, and the data segment of Green. The display time amount of each segment is synchronized by color FOIRU 17 which rotates one time for every frame, and it is made to have data to one color to which DMD14 minded [suitable] color FOIRU 17 displayed. Therefore, time-multiplexing of the data channel to each color (R, G, and B) is carried out so that it may have sequential data to a color with each various frames.
[0024] To the sequential color system 10, the white light is sent through condenser lens 16a from the light source 15, and it converges it one on rotating color FOIRU 17. A color beam of light suits to the size of the mirror array of DMD by 2nd lens 16b. An image is projected on Screen 19 by the reflected light from DMD. The projection lens 18 is adjusted to various screen sizes.
[0025] With reference to drawing 2 and a system 20, data are given along with every one different data paths [three] to three DMD(s)14 about R, G, and B data. The white light is sent through condenser lens 26a from the light source 16, and it converges it through a color filter 27.

Each color filter 26 gives the light (R, G, and B) of a different color to DMD14, and the data to the color are displayed. The image from DMD14 is recombined by filter 26b, and it converges on the projection lens 18, and converges an image to Screen 19. one variation of a system 20 -- one piece -- large-sized -- DMD has the field to each color.

[0026] The comprehensive explanation to both a sequential color like a system 10 and a system 20 and a multi-DMD system is indicated by some patents and patent application which Texas Instruments, Inc. yielded and received. U.S. Pat. No. 5,079,544 "a standard independent digitization video system", U.S. Pat. No. 5,233,385 "white light strengthening color field sequential projection", the United States patent application 07th / No. 678,761 "the DMD architecture used for a pulse-width-modulation display system and timing", the United States patent application 08th / No. 147,249 "a digital television system", and the United States patent application 08th / No. 146,385 "a DMD display system" are contained in it. Such each patent and patent application are incorporated here.

[0027] The description of this invention is recognizing transition energy change arising on a bit plane display. On a bit plane display, segment ** of the sequence of display time amount, i.e., display time amount, is specified by the special data sequence about each bit wait of a pixel. display time amount [as opposed to / as a simple example, can set the sequence over 8 bit pixel data to 7, 6, 5, 4, 3, 2, 1, and 0, and / each bit wait] -- the inside of a frame -- one by one -- short -- **** -- ** Transition energy is related for every transition from one bit level to another bit level. High transition energy can be perceived as artifact.

[0028] One method of reducing a peak energy level "divides" a bit wait, and it is the display time amount over each **** bit wait not being continuous, and making it segmented during a frame period. For example, the display time amount over the most significant bit can be divided to two parts. Next, the data to the most significant bit (MSB) are twice displayed during a frame period, and each of that ON time amount is the one half of the total MSB time amount.

[0029] The display sequence approach which can be used since it supplements with it as a substitute of the bit division approach described above to drawing 3 is shown. By this approach, transition energy is distributed so that the artifact may be reduced.

[0030] This approach is enforced by the multi-SLM system of system 20 grade in the example of drawing 3 . Each DMD14 receives red, Green, or blue data, therefore each is shown as DMD14-R, 14-G, or 14-B.

[0031] As for DMD14 of drawing 3 , memory multiplexing of each is carried out. As described above, this means that data are loaded from the same memory cell as many mirror components. It connects with the reset line by which each mirror components which share a memory cell differ. There is a reset line of a mirror component and the same number per memory cell to Whole DMD. The mirror component connected to the specific reset line is a "reset group." About actuation, after data are loaded to all the memory cells to the reset group of a mirror component, the condition of these mirror components answers and changes to the reset signal on the reset line. It is indicated by/[of the United States patent application which Texas Instruments, Inc. yields about the "split-reset" data loading method accompanying multiplexing and it of memory, and is incorporated here as refer to the receptacle / 08th] No. 300/356 "the pixel control circuit for space optical modulators."

[0032] In the example indicated here, memory multiplexing is based on a low (raw) (it is level), and the fan-out of the mirror component from one memory cell is 4. Therefore, the memory cell of 1 low is shared every 4 lows which a mirror component follows. The mirror component of 4 lows which shares a memory cell is a mirror component of 1 "a block." DMD14 which has the mirror component of 480 lows has the block 41 of 120. Each block 41 has 4 lows and they receive data from the low with the same memory cell.

[0033] Each low is connected to one of four reset lines like the typical memory multiplexing configuration. Although only one reset line 42 is shown, four reset lines are shown in drawing 4 . The reset line 42 is connected to the reset group containing the 1st low of three whole blocks of DMD14. Therefore, the reset group contains one fourth of the low numbers of all DMD(s)14.

[0034] The data to a reset group are loaded in 1 time slice. While the data to the next reset group are loaded, the 1st reset group's mirror component answers a reset signal, and is turned

on and off.
[0035] The reset group who consists of a low which has the block low number more same during data loading of a frame in a detail is loaded by the bit wait in the time slice of a frame period. A "time slice" is a part of frame period, and is a display period over the least significant bit in many cases. Although a time slice is too short and an excessive time slice may not be allowed, generally it is determined by the persistence time of the least significant bit.
[0036] As one example which carries out loading of the data of one frame, and is displayed to up to the memory multiplexing system 20, the 1st reset group's bit n is loaded, then, the 2nd reset group's bit n is loaded, then the 3rd reset group's bit n is loaded, and then the 4th reset group's bit n is loaded. Next, it is continued until the 1st reset group's bit n-1 is loaded, then the 2nd reset group's bit n-1 is loaded and all all reset groups' bit waits are loaded below. Loading of the data to each reset group / bit wait displays front reset group / bit wait data. This example does not necessarily require this, although a bit wait follows the same sequence to each reset group. In fact, in a reset group, various bit wait sequences are advantageous. Thus, all the bit waits [as opposed to the frame in all DMD lows] of data are loaded and displayed through those reset groups during each frame period.
[0037] To the memory multiplexing display system of system 20 grade, special loading and the display pattern which optimize image quality are developed. In the example of drawing 3 , it can consider as the following patterns.
the reset group 1, the bit wait sequence a reset group 2, the bit wait sequence b reset group 3, the bit wait sequence c reset group 4, and the bit wait sequence d — said — as carried out, the bit wait of each sequence is changed among reset groups into loading and De Dis playing.
[0038] DMD14 of drawing 3 has the "corresponding" low, and each n-th low of DMD14 is in the same location about each DMD14. Therefore, the 1st low of the data with which the "1" and 1st [of each DMD14] DMD low which were marked is displayed is received. These three lows are corresponding lows. Similarly, each No. 480 low of DMD14 to 480 low images receives the last low of the data displayed. These three No. 480 lows are corresponding lows.
[0039] The association between the DMD lows and block lows of DMD14 is perpendicularly offset among DMD14 like understanding from drawing. That is, each DMD low is associated with a different block low to 1 set of given corresponding lows of DMD14. For example, the 1st low of DMD14-R is associated with the 1st low of block 41-R (1). However, the 1st low of DMD14-G supports the 4th low of block 41-G (1). The 1st low of DMD14-B supports the 3rd low of block 41-B (1).
[0040] the DMD low which a low and said thing [having carried out] cohere and is associated to the 1st reset group — 1, 5, and 9 of DMD14-R ... 2, 6 and 10 of 477 lows and DMD14-G, and ... 3, 7 and 11 of 478 lows and DMD14-B, and ... they are 479 lows. Each reset pattern is connected by the same pattern, and the DMD low is connected so that there may be no corresponding DMD low into the same reset group.
[0041] As described above, a display is generated by carrying out loading of the reset group of a mirror component, and resetting him. If a specific reset group is displayed, the associated DMD low does not correspond. for example, the DMD low displayed when the reset group connected to the reset line 42 is displayed — 1, 5 and 9 of DMD14-R, and ... 2, 6 and 10 of 477 lows and DMD14-G, and ... 3, 7 and 11 of 478 lows and DMD14-B, and ... they are 479 lows.
[0042] Since association between a corresponding DMD low and a reset group is non-homogeneity, the data to each color can follow the same pattern. However, since the transition times over each color differ, a transition peak is reduced.
[0043] Although said method of making a corresponding DMD low associated with a different reset group is turned to the level memory multiplexing DMD14, the same concept is applicable to other memory multiplexing configurations. For example, memory multiplexing can be made into a vertical angle. The fan-out of each memory cell is a mirror component which follows 1 set of perpendiculars like [in level memory multiplexing]. however, data [as opposed to / the block low meets the diagonal line and / the block low n] — a DMD low — the pixel 1 of 1, and a DMD low — the pixel 4 of 2, and a DMD low — the data to the pixel 3 of 3 and the pixel 2 grade of DMD low 4 may be included There is a block low of 2n-1 to DMD which has n low. Diagonal

memory multiplexing is indicated by the United States patent application 08th incorporated here / No. 300,356 at the detail.
[0044] Drawing 4 shows the 8x8-pixel section of three SLM(s) constituted so that diagonal division reset might be performed according to this invention. There is every four reset line 42 of a to a different reset group. 4 sets of diagonal lows to which SLM14 corresponds are shown. Each matched-pairs angle low of DMD14 is associated with various reset groups.
[0045] The same concept is applied to a system only with two DMD(s). Furthermore, to the single DMD system of system 10 grade, the correspondence between a DMD low and a reset group can be shifted for every color, and can realize the sequential version of the approach of drawing 3 . It can be made the business which reconfigurates a reset group and contains various SLM lows to each color. Since the integral (eye's integration) of an eye is based on the integral of the energy within a frame period, the artifact can be reduced by distributing an energy level appropriately within a frame period.
[0046] Although this invention has been explained about the specific example, this specification does not have constraint-implications. If it is this contractor, various amelioration of not only other examples but the indicated example will be considered to be understanding with it being easy. Therefore, all amelioration that enters within the limits of the truth of invention shall go into a claim.
[0047] The following terms are further indicated about the above explanation.
(1) Have the memory multiplexing space optical modulator (SLM) of . large number, and the image based on the pixel data showing each color from which SLM differs is displayed. An image is the artifact reduction approach in the image display system combined in an image plane. This approach The step which identifies the SLM low which identifies said low of SLM which has a low location [/ in said SLM], and corresponds, each reset group -- said every -- there is no SLM low which consists of some lows of SLM and moreover corresponds into the same reset group -- as -- the inside of a reset group -- said every -- with the step which connects the low of SLM The step which loads the data which have a certain bit wait of said pixel data to the 1st reset group, The step which displays said data loaded to said 1st reset group, The artifact reduction approach which consists of a step which repeats said loading step and said display step by turns among said reset groups about each reset group and each bit wait of said pixel data.
[0048] (2) The artifact reduction approach in the reset group from whom it is an approach given in . 1st term, and said each low of a corresponding low differs.
[0049] (3) It is the artifact reduction approach enforced so that it may be an approach given in . 1st term and said repeat step may be loaded in various sequence to a reset group with said various bit waits.
[0050] (4) It is the artifact reduction approach which it is an approach given in . 1st term, and said loading step and said display step are carried out within two continuous time slices of a frame period, and is determined by the display time amount over the data with which said time slice has a least significant bit wait substantially.
[0051] (5) It is the artifact reduction approach which is a thing [as opposed to / are an approach given in . 1st term, and / one / of said the SLM display data / to two colors / the 3rd color in one of said the SLM data].
[0052] (6) The artifact reduction approach which is an approach given in . 1st term, and is a thing to the color from which said each SLM display data differs.
[0053] (7) It is the artifact reduction approach that it is an approach given in . 1st term, and said SLM is a digital micro mirror device.
[0054] (8) It is the artifact reduction approach that are an approach given in . 1st term, and said corresponding low meets said level low of SLM, and a reset group contains said level low.
[0055] (9) It is the artifact reduction approach that are an approach given in . 1st term, and said corresponding low meets said diagonal low of SLM, and said reset group contains said diagonal low.
[0056] (10) Have . memory multiplexing space optical modulator (SLM), and color FOIRU is minded. It is the artifact reduction approach in an image display system which displays serially

the image based on the pixel data showing a different color. This approach The step which assigns a reset group said low of SLM so that each reset group may consist of said some of lows of SLM, The step which loads the data which have a certain bit wait of said pixel data to the 1st reset group, The step which displays said data loaded to said 1st reset group, The step which repeats said loading step and said display step by turns among said reset groups about each reset group and each bit wait of said pixel data of the 1st color, The artifact reduction approach which assigns and consists of said loading and step which repeats a display step about said pixel data of the 2nd color so that said reset group may contain said various lows of SLM.

[0057] (11) It is the artifact reduction approach enforced so that it may be an approach given in . 10th term and said repeat step may be loaded in various sequence to a reset group with said various bit waits.

[0058] (12) It is the artifact reduction approach which it is an approach given in . 10th term, and said loading step and said display step are carried out within two continuous time slices of a frame period, and is determined by the display time amount over the data with which said time slice has a least significant bit wait substantially.

[0059] (13) It is the artifact reduction approach that are an approach given in . 10th term, and said reset group contains said diagonal low of SLM.

[0060] (14) It is the artifact reduction approach that are an approach given in . 10th term, and said reset group contains said level low of SLM.

[0061] (15) It is the artifact reduction approach that it is an approach given in . 10th term, and said SLM is a digital micro mirror device.

[0062] (16) It is the display system 10 based on .SLM, and the artifact reduction approach in 20, and the image is based on the data displayed by the bit wait to the level on the strength by which pulse width modulation was carried out. This approach can be used for the single SLM system 10 which generates the image of various colors serially during the multi-SLM system 20 which displays the image of various colors in coincidence, or each frame period. To the multi-SLM system 20, this approach is used for SLM14 which has the "reset group" by whom memory multiplexing was done, and who is loaded to various time amount and displayed. The low to which SLM corresponds is various reset groups and eclipse ****** with association.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the artifact reduction approach in the display system which generates a color display especially using one or more space optical modulators about an image display system.

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PRIOR ART

[Description of the Prior Art] It is gradually used as what the image display system based on a space optical modulator (SLM:spatial light modolator) replaces with the image display system based on a cathode-ray tube. SLM used for image display application is a pixel generating component array which emits or reflects light in an image plane. It discriminates from a pixel and the pixel generating component itself is called a "pixel" in many cases. If it turns out that two or more pixels of a SLM array can be used for generating one pixel, this vocabulary is obvious from a context.
[0003] A digital micro mirror device (DMD:digital micro-mirror device) is one sort of SLM. DMD has the array of hundreds thru/or thousands of small inclination mirrors. Since it enables it to incline, each mirror is attached in one or more hinges laid in the stanchion, and spacing is taken by the opening from the lower layer control circuit. A control circuit gives electrostatic force and, thereby, each mirror inclines alternatively. The reinforcement of 1 pixel is given by each mirror component.
[0004] The address of the mirror component of DMD can be carried out according to an individual so that an image may be demarcated by which pixel is turned on and off to given time amount. In order to carry out the address of the mirror component of DMD, each mirror component is connected with the memory cell which memorizes a little data which determine the on-off condition of an address signal. Addressing is binary at the point that the address of each mirror component is carried out by the yes or low signal which shows whether a mirror component reflects light in an image plane. DMD "is loaded" by memorizing input data in a memory cell through the data loading circuit of the DMD array circumference of a mirror component.
[0005] Pixel data are sent to the memory cell of DMD in a space "bit plane (bit-plane)" format. In this format, data are arranged by the bit wait (bit-weight) of every pixel and all pixels to each frame. In this format, a gray scale image can be generated by carrying out the address of each mirror component during an one-frame period with the consecutive-addresses signal with which each expresses the bit wait from which the n bit pixel value of that mirror component differs. The time amount it is supposed that a mirror component continues being ON becomes long, so that the bit wait of the bit used for addressing is a high order. To the brightest reinforcement, whenever the address of the mirror component is carried out, it is set to ON. This is essentially pulse width modulation and many variations are possible for it. A migration image can be generated by carrying out the re-address of the DMD with the data to a continuous frame.
[0006] One approach for a color image is using three DMD(s) per piece about each primary color (R, G, B). It converges the light from each pixel to which DMD corresponds so that an observer may perceive a desired color. Another approach is using the color wheel (color wheel) which has one DMD and primary color partition. It is made to be unified to the color image with which the sequence of the data to various colors is carried out, they are synchronized to a color wheel, and a sequential image continues in an eye. By the 3rd approach, two DMD(s) are used, one side is used for the change between 2 colors, and it is used for another side displaying the 3rd color.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] With any display systems, although that is right, the quality of the image from a DMD base display system improves by canceling the artifact. When an observer winks to the potential artifact, an eye is moved or a hand is shaken in front of an eye, a temporary border line which appears as a flash plate or a muscle is contained. Another artifact is a motion border line, and it appears as a false border line, when having run after the migration body by the eye. A false border line is a ghost image in a steep edge, or an artifact border line in the field which changes gently. There is also artifact of other type peculiar to the DMD display system which uses the data loading method learned as memory multiplexing.

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MEANS

[Means for Solving the Problem] One description of this invention is the artifact reduction approach in the image display system which has many memory multiplexing space optical modulators (SLM). In this kind of system, each SLM displays the image based on the data showing a different color in coincidence, and an image is combined in an image plane. SLM has a "corresponding" SLM low (raw) and it is a low which has a low corresponding location. For memory multiplexing, the low of SLM is connected within the reset group. Each reset group consists of some of each lows of SLM, and there is no corresponding SLM low into the same reset group. While carrying out loading of the data to SLM, the data which have a certain bit wait of pixel data are loaded to the 1st reset group. This data is displayed while the data which have a certain bit wait of pixel data are loaded to the next reset group. These loading and a display step are repeated to each reset group and each bit wait of pixel data.
[0009] Since the advantage of this invention does not contain the SLM low to which a reset group corresponds, it is that the artifact by the periodicity of a split reset configuration is reduced. For example, if the split reset configuration is level, the inclination to perceive horizontal line structure will decrease.
[0010] This invention is useful also to the single SLM system which displays serially the image of various colors which minded the color wheel using one SLM. In this case, there are only 1 set of SLM lows. The reset group to one color has a different low from the reset group to another color.
[0011]
[Embodiment of the Invention] Drawing 1 and drawing 2 are the block diagrams of the color display systems 10 and 20 based on SLM, respectively. The system 10 is using one SLM which displays the image of various colors through a color wheel serially. A system 20 uses three SLM (s) and the each displays in coincidence the data to the color from which an image differs. Irrespective of whether a color display is serially given like a system 10, or it is given to coincidence like a system 20, each system has many data channels and is made into the colors from which each channel differs so that a postscript may be carried out. Generally, this invention reduces the artifact in the image displayed by changing the timing of the data of various channels.
[0012] For example, SLM14 of a system 10 and SLM14 of a system 20 are the DMD molds SLM. In this invention, the memory multiplexing SLM is used so that a postscript may be carried out. When SLM is DMD, this memory multiplexing is enabled by the latching property of the inclination mirror it is supposed that is set as ON or an off position until it is reset. With this property, when 1 set of mirror components are already set up, 1 more set of mirror components can be loaded to a related memory cell. Thereby, a mirror component can share a memory cell.
[0013] The image signal which a system 10 and a system 20 receive can be made into the analog signal changed into a digital format in a digital signal or the back. For example, a conversion number can be considered to be an analog signal like the broadcast television signal.
[0014] Only the component important for the main screen processing is shown in drawing 1 and drawing 2 . Other components used for functions, such as synchronization and processing of an audio signal, and closed KYAPUSHONINGU (closed captioning), are not shown.

[0015] A system 10 and a system 20 have the same configuration as a "front end" component, and contain the signal interface 11, the processing system 12, and frame memory 13 for giving digital image data to DMD14. These components are examined in common to a system 10 and a system 20, and the optical system to which DMD14 and two systems relate is examined separately. In examining a system 10 and a system 20 in common, DMD expresses much DMD14 of one DMD of a system 10, or a system 20.
[0016] The signal interface 11 receives an analog input signal, and divides it into a video signal, a synchronizing signal, and an audio signal. The signal interface 11 contains the A/D converter and color separator which change a signal into pixel data and separate brightness data from chrominance data, respectively. In the another example, before color separation performs A/D conversion, it is performed using an analog filter.
[0017] The processor system 12 prepares the pixel data displayed by carrying out various pixel processing tasks. The processor system 12 contains various memory devices, such as the field, a line buffer, etc. which store pixel data during processing.
[0018] One task typically carried out by the processor system 12 is advance scan conversion of the interlaced data, and each field of the interlaced data is changed into a perfect frame. Other processing tasks are a scaling, a color space conversion, or a gamma correction. Brightness and chrominance data are changed into RGB data into a color space conversion. Since gamma compensation becomes unnecessary with the linearity property of DMD14, the data in which gamma compensation was carried out by the gamma correction are reverse-compensated.
[0019] In the example, the processor system 12 contains the "scanning-line video processor" which carries out computation tasks, such as advance scan conversion and a scaling. This device is marketed from Texas Instruments, Inc., and can perform line BAIRAIN processing of pixel data.
[0020] A frame memory 13 receives the pixel data processed from the processor system 12. In an input or an output, a frame memory 13 changes data into a "bit plane" format, and sends bit plane data to DMD. As the Prior art examined, a bit plane format is a format pixel data are reconfigurated by whose bit wait. Thereby, each pixel of DMD14 can answer the value of 1 bit data of a certain time amount, and can be turned on and off.
[0021] With the typical display system 10, a frame memory 13 is "double buffer" memory, and it means having the capacity to at least two display frames. While writing in the buffer to one display frame, the buffer to the display frame of another side can be read to DMD14. Two buffers can be controlled at a "ping-pong" ceremony, and DMD14 can obtain data continuously.
[0022] As described above by the Prior art, DMD14 is a binary device which has the on-off condition of each mirror component. The bit plane to each bit of data is loaded by the pulse-width-modulation sequence, and is displayed. To n bit pixel data, there is an n bit plane per frame period. During a frame period, an observer unifies binary data and perceives various reinforcement of the image of the frame.
[0023] Next, one color is given at a stretch to each frame of the RGB data to DMD14, and it is made to be divided in each frame of data with reference to drawing 1 and a system 10 to red, blue, and the data segment of Green. The display time amount of each segment is synchronized by color FOIRU 17 which rotates one time for every frame, and it is made to have data to one color to which DMD14 minded [suitable] color FOIRU 17 displayed. Therefore, time-multiplexing of the data channel to each color (R, G, and B) is carried out so that it may have sequential data to a color with each various frames.
[0024] To the sequential color system 10, the white light is sent through condenser lens 16a from the light source 15, and it converges it one on rotating color FOIRU 17. A color beam of light suits to the size of the mirror array of DMD by 2nd lens 16b. An image is projected on Screen 19 by the reflected light from DMD. The projection lens 18 is adjusted to various screen sizes.
[0025] With reference to drawing 2 and a system 20, data are given along with every one different data paths [three] to three DMD(s)14 about R, G, and B data. The white light is sent through condenser lens 26a from the light source 16, and it converges it through a color filter 27. Each color filter 26 gives the light (R, G, and B) of a different color to DMD14, and the data to

the color are displayed. The image from DMD14 is recombined by filter 26b, and it converges on the projection lens 18, and converges an image to Screen 19. one variation of a system 20 -- one piece -- large-sized -- DMD has the field to each color.
[0026] The comprehensive explanation to both a sequential color like a system 10 and a system 20 and a multi-DMD system is indicated by some patents and patent application which Texas Instruments, Inc. yielded and received. U.S. Pat. No. 5,079,544 "a standard independent digitization video system", U.S. Pat. No. 5,233,385 "white light strengthening color field sequential projection", the United States patent application 07th / No. 678,761 "the DMD architecture used for a pulse-width-modulation display system and timing", the United States patent application 08th / No. 147,249 "a digital television system", and the United States patent application 08th / No. 146,385 "a DMD display system" are contained in it. Such each patent and patent application are incorporated here.
[0027] The description of this invention is recognizing transition energy change arising on a bit plane display. On a bit plane display, segment ** of the sequence of display time amount, i.e., display time amount, is specified by the special data sequence about each bit wait of a pixel. display time amount [as opposed to / as a simple example, can set the sequence over 8 bit pixel data to 7, 6, 5, 4, 3, 2, 1, and 0, and / each bit wait] -- the inside of a frame -- one by one -- short -- **** -- ** Transition energy is related for every transition from one bit level to another bit level. High transition energy can be perceived as artifact.
[0028] One method of reducing a peak energy level "divides" a bit wait, and it is the display time amount over each **** bit wait not being continuous, and making it segmented during a frame period. For example, the display time amount over the most significant bit can be divided to two parts. Next, the data to the most significant bit (MSB) are twice displayed during a frame period, and each of that ON time amount is the one half of the total MSB time amount.
[0029] The display sequence approach which can be used since it supplements with it as a substitute of the bit division approach described above to drawing 3 is shown. By this approach, transition energy is distributed so that the artifact may be reduced.
[0030] This approach is enforced by the multi-SLM system of system 20 grade in the example of drawing 3 . Each DMD14 receives red, Green, or blue data, therefore each is shown as DMD14-R, 14-G, or 14-B.
[0031] As for DMD14 of drawing 3 , memory multiplexing of each is carried out. As described above, this means that data are loaded from the same memory cell as many mirror components. It connects with the reset line by which each mirror components which share a memory cell differ. There is a reset line of a mirror component and the same number per memory cell to Whole DMD. The mirror component connected to the specific reset line is a "reset group." About actuation, after data are loaded to all the memory cells to the reset group of a mirror component, the condition of these mirror components answers and changes to the reset signal on the reset line. It is indicated by/[of the United States patent application which Texas Instruments, Inc. yields about the "split-reset" data loading method accompanying multiplexing and it of memory, and is incorporated here as refer to the receptacle / 08th] No. 300/356 "the pixel control circuit for space optical modulators."
[0032] In the example indicated here, memory multiplexing is based on a low (raw) (it is level), and the fan-out of the mirror component from one memory cell is 4. Therefore, the memory cell of 1 low is shared every 4 lows which a mirror component follows. The mirror component of 4 lows which shares a memory cell is a mirror component of 1 "a block." DMD14 which has the mirror component of 480 lows has the block 41 of 120. Each block 41 has 4 lows and they receive data from the low with the same memory cell.
[0033] Each low is connected to one of four reset lines like the typical memory multiplexing configuration. Although only one reset line 42 is shown, four reset lines are shown in drawing 4 . The reset line 42 is connected to the reset group containing the 1st low of three whole blocks of DMD14. Therefore, the reset group contains one fourth of the low numbers of all DMD(s)14.
[0034] The data to a reset group are loaded in 1 time slice. While the data to the next reset group are loaded, the 1st reset group's mirror component answers a reset signal, and is turned on and off.

[0035] The reset group who consists of a low which has the block low number more same during data loading of a frame in a detail is loaded by the bit wait in the time slice of a frame period. A "time slice" is a part of frame period, and is a display period over the least significant bit in many cases. Although a time slice is too short and an excessive time slice may not be allowed, generally it is determined by the persistence time of the least significant bit.
[0036] As one example which carries out loading of the data of one frame, and is displayed to up to the memory multiplexing system 20, the 1st reset group's bit n is loaded, then, the 2nd reset group's bit n is loaded, then the 3rd reset group's bit n is loaded, and then the 4th reset group's bit n is loaded. Next, it is continued until the 1st reset group's bit n-1 is loaded, then the 2nd reset group's bit n-1 is loaded and all all reset groups' bit waits are loaded below. Loading of the data to each reset group / bit wait displays front reset group / bit wait data. This example does not necessarily require this, although a bit wait follows the same sequence to each reset group. In fact, in a reset group, various bit wait sequences are advantageous. Thus, all the bit waits [as opposed to the frame in all DMD lows] of data are loaded and displayed through those reset groups during each frame period.
[0037] To the memory multiplexing display system of system 20 grade, special loading and the display pattern which optimize image quality are developed. In the example of drawing 3 , it can consider as the following patterns.
the reset group 1, the bit wait sequence a reset group 2, the bit wait sequence b reset group 3, the bit wait sequence c reset group 4, and the bit wait sequence d -- said -- as carried out, the bit wait of each sequence is changed among reset groups into loading and De Dis playing.
[0038] DMD14 of drawing 3 has the "corresponding" low, and each n-th low of DMD14 is in the same location about each DMD14. Therefore, the 1st low of the data with which the "1" and 1st [of each DMD14] DMD low which were marked is displayed is received. These three lows are corresponding lows. Similarly, each No. 480 low of DMD14 to 480 low images receives the last low of the data displayed. These three No. 480 lows are corresponding lows.
[0039] The association between the DMD lows and block lows of DMD14 is perpendicularly offset among DMD14 like understanding from drawing. That is, each DMD low is associated with a different block low to 1 set of given corresponding lows of DMD14. For example, the 1st low of DMD14-R is associated with the 1st low of block 41-R (1). However, the 1st low of DMD14-G supports the 4th low of block 41-G (1). The 1st low of DMD14-B supports the 3rd low of block 41-B (1).
[0040] the DMD low which a low and said thing [having carried out] cohere and is associated to the 1st reset group -- 1, 5, and 9 of DMD14-R ... 2, 6 and 10 of 477 lows and DMD14-G, and ... 3, 7 and 11 of 478 lows and DMD14-B, and ... they are 479 lows. Each reset pattern is connected by the same pattern, and the DMD low is connected so that there may be no corresponding DMD low into the same reset group.
[0041] As described above, a display is generated by carrying out loading of the reset group of a mirror component, and resetting him. If a specific reset group is displayed, the associated DMD low does not correspond. for example, the DMD low displayed when the reset group connected to the reset line 42 is displayed -- 1, 5 and 9 of DMD14-R, and ... 2, 6 and 10 of 477 lows and DMD14-G, and ... 3, 7 and 11 of 478 lows and DMD14-B, and ... they are 479 lows.
[0042] Since association between a corresponding DMD low and a reset group is non-homogeneity, the data to each color can follow the same pattern. However, since the transition times over each color differ, a transition peak is reduced.
[0043] Although said method of making a corresponding DMD low associated with a different reset group is turned to the level memory multiplexing DMD14, the same concept is applicable to other memory multiplexing configurations. For example, memory multiplexing can be made into a vertical angle. The fan-out of each memory cell is a mirror component which follows 1 set of perpendiculars like [in level memory multiplexing]. however, data [as opposed to / the block low meets the diagonal line and / the block low n] -- a DMD low -- the pixel 1 of 1, and a DMD low -- the pixel 4 of 2, and a DMD low -- the data to the pixel 3 of 3 and the pixel 2 grade of DMD low 4 may be included There is a block low of 2n-1 to DMD which has n low. Diagonal memory multiplexing is indicated by the United States patent application 08th incorporated

here / No.300,356 at the detail.
[0044] Drawing 4 shows the 8x8-pixel section of three SLM(s) constituted so that diagonal division reset might be performed according to this invention. There is every four reset line 42 of a to a different reset group. 4 sets of diagonal lows to which SLM14 corresponds are shown. Each matched-pairs angle low of DMD14 is associated with various reset groups.
[0045] The same concept is applied to a system only with two DMD(s). Furthermore, to the single DMD system of system 10 grade, the correspondence between a DMD low and a reset group can be shifted for every color, and can realize the sequential version of the approach of drawing 3 . It can be made the business which reconfigurates a reset group and contains various SLM lows to each color. Since the integral (eye's integration) of an eye is based on the integral of the energy within a frame period, the artifact can be reduced by distributing an energy level appropriately within a frame period.
[0046] Although this invention has been explained about the specific example, this specification does not have constraint-implications. If it is this contractor, various amelioration of not only other examples but the indicated example will be considered to be understanding with it being easy. Therefore, all amelioration that enters within the limits of the truth of invention shall go into a claim.
[0047] The following terms are further indicated about the above explanation.
(1) Have the memory multiplexing space optical modulator (SLM) of . large number, and the image based on the pixel data showing each color from which SLM differs is displayed. An image is the artifact reduction approach in the image display system combined in an image plane. This approach The step which identifies the SLM low which identifies said low of SLM which has a low location [/ in said SLM], and corresponds, each reset group — said every — there is no SLM low which consists of some lows of SLM and moreover corresponds into the same reset group — as — the inside of a reset group — said every — with the step which connects the low of SLM The step which loads the data which have a certain bit wait of said pixel data to the 1st reset group, The step which displays said data loaded to said 1st reset group, The artifact reduction approach which consists of a step which repeats said loading step and said display step by turns among said reset groups about each reset group and each bit wait of said pixel data.
[0048] (2) The artifact reduction approach in the reset group from whom it is an approach given in . 1st term, and said each low of a corresponding low differs.
[0049] (3) It is the artifact reduction approach enforced so that it may be an approach given in . 1st term and said repeat step may be loaded in various sequence to a reset group with said various bit waits.
[0050] (4) It is the artifact reduction approach which it is an approach given in . 1st term, and said loading step and said display step are carried out within two continuous time slices of a frame period, and is determined by the display time amount over the data with which said time slice has a least significant bit wait substantially.
[0051] (5) It is the artifact reduction approach which is a thing [as opposed to / are an approach given in . 1st term, and / one / of said the SLM display data / to two colors / the 3rd color in one of said the SLM data].
[0052] (6) The artifact reduction approach which is an approach given in . 1st term, and is a thing to the color from which said each SLM display data differs.
[0053] (7) It is the artifact reduction approach that it is an approach given in . 1st term, and said SLM is a digital micro mirror device.
[0054] (8) It is the artifact reduction approach that are an approach given in . 1st term, and said corresponding low meets said level low of SLM, and a reset group contains said level low.
[0055] (9) It is the artifact reduction approach that are an approach given in . 1st term, and said corresponding low meets said diagonal low of SLM, and said reset group contains said diagonal low.
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[0057] (11) It is the artifact reduction approach enforced so that it may be an approach given in . 10th term and said repeat step may be loaded in various sequence to a reset group with said various bit waits.
[0058] (12) It is the artifact reduction approach which it is an approach given in . 10th term, and said loading step and said display step are carried out within two continuous time slices of a frame period, and is determined by the display time amount over the data with which said time slice has a least significant bit wait substantially.
[0059] (13) It is the artifact reduction approach that are an approach given in . 10th term, and said reset group contains said diagonal low of SLM.
[0060] (14) It is the artifact reduction approach that are an approach given in . 10th term, and said reset group contains said level low of SLM.
[0061] (15) It is the artifact reduction approach that it is an approach given in . 10th term, and said SLM is a digital micro mirror device.
[0062] (16) It is the display system 10 based on .SLM, and the artifact reduction approach in 20, and the image is based on the data displayed by the bit wait to the level on the strength by which pulse width modulation was carried out. This approach can be used for the single SLM system 10 which generates the image of various colors serially during the multi-SLM system 20 which displays the image of various colors in coincidence, or each frame period. To the multi-SLM system 20, this approach is used for SLM14 which has the "reset group" by whom memory multiplexing was done, and who is loaded to various time amount and displayed. The low to which SLM corresponds is various reset groups and eclipse ****** with association.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram of the SLM base display system which gives a color image using one SLM and color FOIRU.
[Drawing 2] The block diagram of the display system based on SLM which gives a color image using much SLM(s).
[Drawing 3] Drawing showing how to reduce the artifact in the system of drawing 2 which has the level memory multiplexing SLM.
[Drawing 4] Drawing showing the approach for SLM by which memory multiplexing is carried out at a vertical angle.
[Description of Notations]
10 20 Color display system based on SLM
11 Signal Interface
12 Processing System
13 Frame Memory
14, 14R, 14-B, 14-G Digital mirror device
15 Light Source
16a, 16b Lens
17 Color FOIRU
18 Projection Lens
19 Screen
26a, 26b Condenser lens
27 Color Filter

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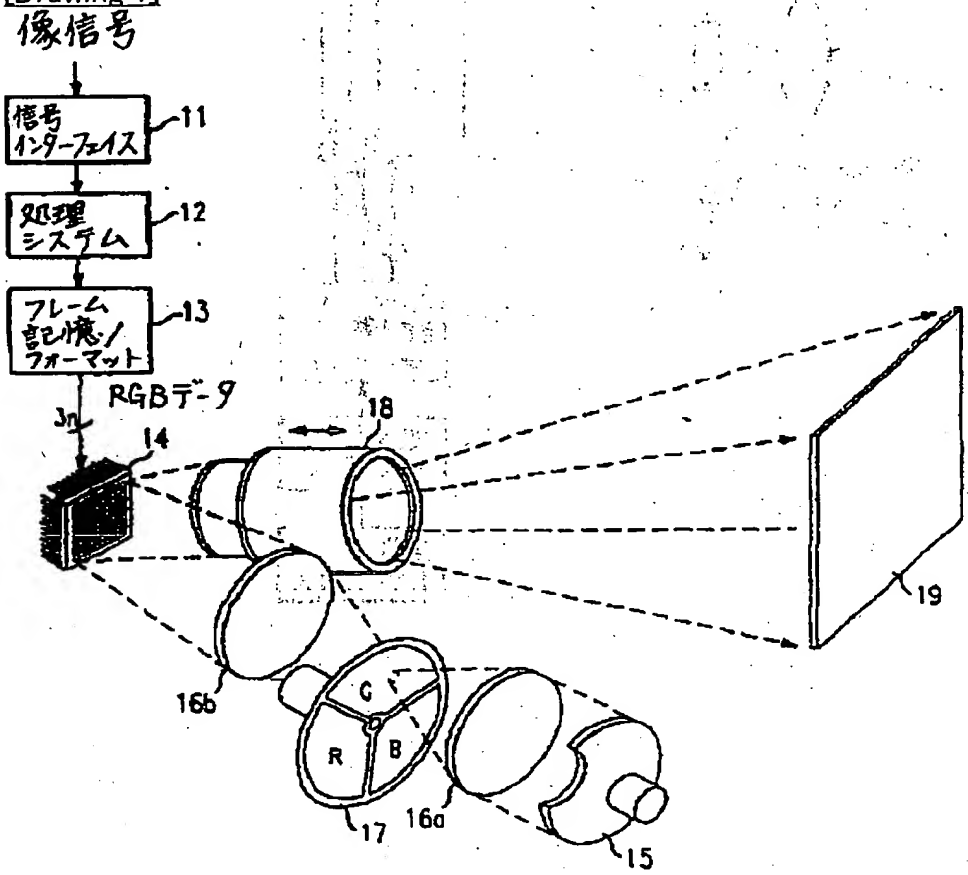
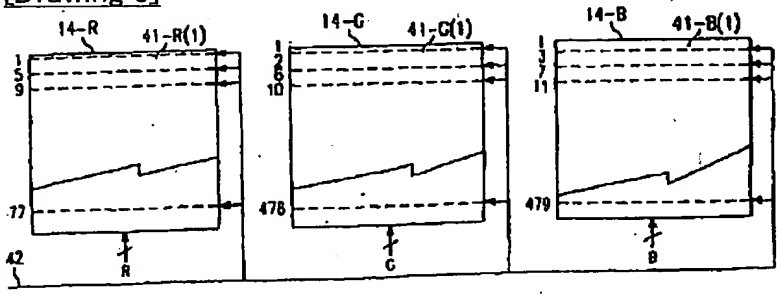
DRAWINGS

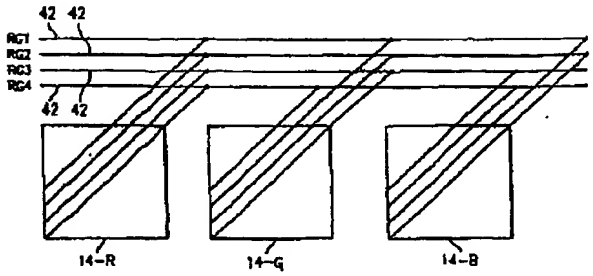
[Drawing 1]



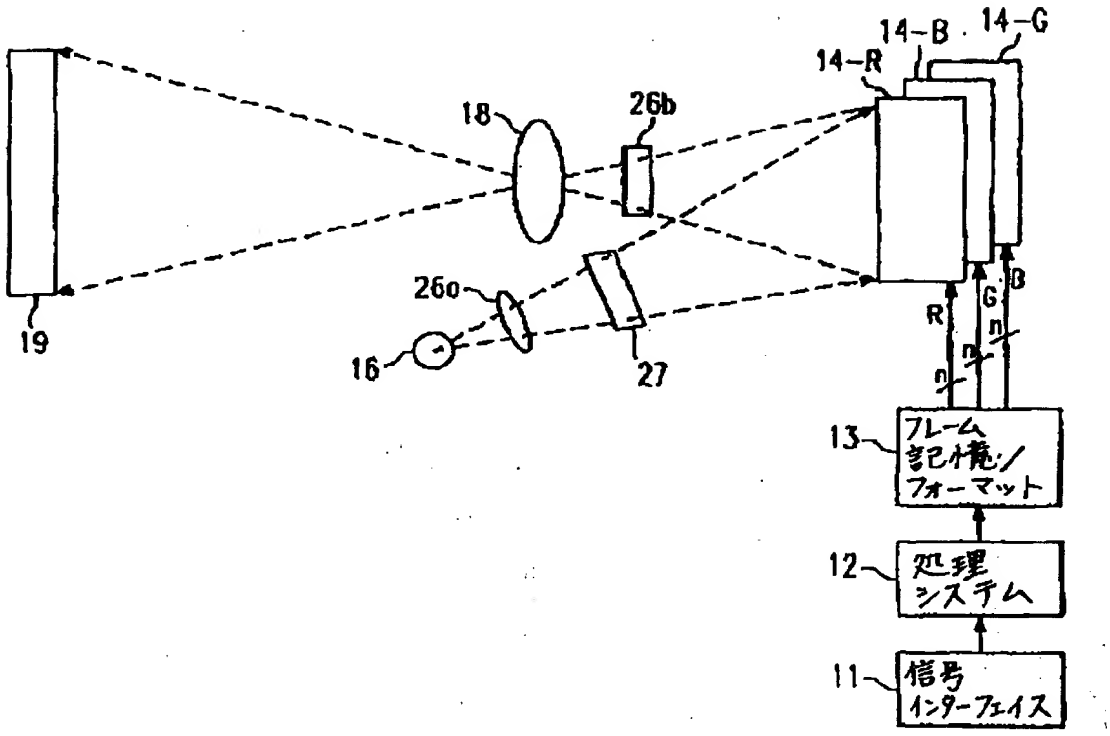
[Drawing 3]



[Drawing 4]



[Drawing 2]



[Translation done.]